first etching said damascene opening through said dielectric layer to said liner layer overlying said contact region wherein said first etching comprises a high F/C ratio etch chemistry, high power, and low pressure; and

second etching said liner layer within said damascene opening to expose said contact region wherein said second etching comprises a high F/C ratio etch chemistry, low power, and low pressure to complete formation of said damascene opening in said fabrication of said integrated circuit device.

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2. (AMENDED) The method according to Claim 1 wherein said contact region is a gate electrode, a source region, a drain region, or a metal line.

3. (AMENDED) The method according to Claim 1 wherein said liner layer is silicon nitride or silicon carbide and has a thickness of between about 300 and 700 Angstroms.

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5. (AMENDED) The method according to Claim 1 wherein said dielectric layer is Black Diamond or organic

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dielectric materials and has a thickness of between about 6000 and 10,000 Angstroms.

14. (AMENDED) The method according to Claim 13 wherein said metal layer is copper or aluminum-copper alloys.

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15. (AMENDED) A method of forming a damascene opening in the fabrication of an integrated circuit device comprising:

providing a contact region in or on a substrate;

depositing a liner layer overlying said contact region;

depositing a dielectric layer overlying said liner layer wherein said dielectric layer has a dielectric constant of less than 2.5 and wherein no etch stop layer is used within said dielectric layer;

first etching said damascene opening through said dielectric layer to said liner layer overlying said region to be contacted wherein said first etching comprises a high F/C ratio etch chemistry, power of between 700 and 1000 watts, and pressure of between 20 and 150 mTorr; and

second etching said liner layer within said damascene opening to expose said region to be contacted wherein said second etching comprises a high F/C ratio

etch chemistry, power of between 250 and 500 watts, and pressure of between 30 and 70 mTorr to complete formation of said damascene opening in said fabrication of said integrated circuit device.

16. (AMENDED) The method according to Claim 15 wherein said contact region is a gate electrode, a source region, a drain regions, or a metal line.

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17. (AMENDED) The method according to Claim 15 wherein said liner layer is silicon nitride or silicon carbide and has a thickness of between about 300 and 700 Angstroms.

18. (AMENDED) The method according to Claim 15 wherein said dielectric layer is Black Diamond or organic dielectric materials and has a thickness of between about 6000 and 10,000 Angstroms.

23. (AMENDED) The method according to Claim 22 wherein said metal layer is copper or aluminum-copper alloys.

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24. (AMENDED) A method of copper metallization in the fabrication of an integrated circuit device comprising:

providing a contact region in or on a substrate;

depositing a liner layer overlying said contact region;

depositing a dielectric layer overlying said liner layer wherein said dielectric layer has a dielectric constant of less than 2.5;

first etching said damascene opening through said dielectric layer to said liner layer overlying said region to be contacted wherein said first etching comprises a high F/C ratio etch chemistry of CF_4, O_2, and Ar gases, power of between 700 and 1000 watts, and pressure of between 20 and 150 mTorr;

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second etching said liner layer within said damascene opening to expose said region to be contacted wherein said second etching comprises a high F/C ratio etch chemistry, power of between 250 and 500 watts, and pressure of between 30 and 70 mTorr;

depositing a barrier metal layer within said damascene opening;

depositing a copper layer overlying said barrier metal layer; and

polishing down said copper layer and said barrier metal layer to leave said barrier metal layer and said copper layer only within said damascene opening to complete said copper metallization in said fabrication of said integrated circuit device.

25. (AMENDED) The method according to Claim 24 wherein said contact region is a gate electrode, a source region, a drain regions, or a metal line.

26. (AMENDED) The method according to Claim 24 wherein said liner layer is silicon nitride or silicon carbide and has a thickness of between about 300 and 700 Angstroms.

A5 end

27. (AMENDED) The method according to Claim 24 wherein said dielectric layer is Black Diamond or organic dielectric materials and has a thickness of between about 6000 and 10,000 Angstroms.

REMARKS

Examiner K. Chen is thanked for the thorough examination and search of the subject Patent Application. Claims 1-3, 5, 14-18, 23, and 24 have been amended and Claim 4 has been cancelled.

The Specification has been amended to correct a typing error in the Patent number of a reference.